MONASH University
Information Technology

FIT2069
Computer architecture

Unit Guide

Semester 1, 2011

Last updated: 27 Feb 2011

Table of Contents

FIT2069 Computer architecture - Semester 1, 2011

This unit covers the internal mechanism of computers and how they are organised and programmed. Topics include combinatorial and sequential logic, Boolean Algebra, Karnaugh maps, counters, ripple adders, tree adders, memory/addressing, busses, speed, DMA, data representation, machine arithmetic, microprogramming, caches and cache architectures, virtual memory and translation look-aside buffers, vectored interrupts, polled interrupts, pipelined architecture, superscalar architecture, data dependency, hazards, CISC, RISC, VLIW machine architectures.

Mode of Delivery

Clayton (Day)

Contact Hours

2 hrs lectures/wk, 3 hr laboratory/fortnight, 1 hr tutorial/fortnight

Workload

- Lectures: 2 hrs per week
- Laboratory: 3 hrs per fortnight
- Tutorial: 1 hr per fortnight

This is a technically oriented unit where content in any given week depends strongly on content in preceding weeks. Therefore students should plan and commit a minimum of 8 to 12 hours for personal study every week and should allocate up to 5 hours per week in some weeks for use of a computer. Laboratory work will require preparation before attendance.

The unit content requires a strong focus on understanding content through the semester.

Unit Relationships

Prerequisites

FIT1031 or FIT1001 and FIT1008 or FIT1015

Chief Examiner

Carlo Kopp

Campus Lecturer

Clayton

Dr Carlo Kopp

Contact hours: By appointment / email (part time staff)

Learning Objectives

At the completion of this unit students will have -
A knowledge and understanding of:

- combinatorial and sequential logic, Boolean Algebra, Karnaugh maps, and hazards;
- counters, ripple adders, tree adders, memory/addressing, computer busses, logic and bus speed, and Direct Memory Access;
- data representation for integers and floating point operands;
- machine arithmetic, microprogramming;
- storage herarchies, caches and cache architectures, performance impact of caching;
- virtual memory and translation look-aside buffers, performance impact of TLB caching;
- vectored and polled interrupt handling;
- pipelined architecture, superscalar architecture, data dependency, and hazards;
- CISC, RISC, VLIW machine architectures.

Developed the skills to:

- model combinatorial and sequential logic circuits using a simulator tool;
- perform programming tasks in assembly code.

Graduate Attributes

Monash prepares its graduates to be:

1. responsible and effective global citizens who:

a. engage in an internationalised world
b. exhibit cross-cultural competence
c. demonstrate ethical values

critical and creative scholars who:

a. produce innovative solutions to problems
b. apply research skills to a range of challenges
c. communicate perceptively and effectively

Assessment Summary

Examination (3 hours): 60%; In-semester assessment: 40%

Assessment Task	Value	Due Date
Laboratory Exercises	5% of total mark each	In weeks 2,4,6,8,10 and 12
Tutorial Exercises	Total 10%; 1.667% each	In weeks 1,3,5,7,9 and 11
Examination 1	60%	To be advised

Teaching Approach

- **Lecture and tutorials or problem classes**
  This teaching and learning approach provides facilitated learning, practical exploration and peer learning.
- **Laboratory-based classes**
  This teaching approach is practical learning.

Feedback

Our feedback to You

Types of feedback you can expect to receive in this unit are:

- Informal feedback on progress in labs/tutes
- Test results and feedback

Your feedback to Us

Monash is committed to excellence in education and regularly seeks feedback from students, employers and staff. One of the key formal ways students have to provide feedback is through SETU, Student Evaluation of Teacher and Unit. The University's student evaluation policy requires that every unit is evaluated each year. Students are strongly encouraged to complete the surveys. The feedback is anonymous and provides the Faculty with evidence of aspects that students are satisfied and areas for improvement.

For more information on Monash's educational strategy, and on student evaluations, see:
http://www.monash.edu.au/about/monash-directions/directions.html
http://www.policy.monash.edu/policy-bank/academic/education/quality/student-evaluation-policy.html

Previous Student Evaluations of this unit

If you wish to view how previous students rated this unit, please go to
https://emuapps.monash.edu.au/unitevaluations/index.jsp

Recommended Resources

Logisim software (free)

Xspim/Spim software (free)

Examination material or equipment

Non-programmable scientific calculators will be permitted.

Unit Schedule

Week	Date*	Activities	Assessment
0	21/02/11		No formal assessment or activities are undertaken in week 0
1	28/02/11	Intro/History/Background; Boolean Algebra	Tutorial
2	07/03/11	Karnaugh maps, Hazards; Data Representation	Laboratory
3	14/03/11	Counters, Adders, Shifters, Sequential Logic	Tutorial
4	21/03/11	Basic Machine Organisation	Laboratory
5	28/03/11	Control Unit Design	Tutorial
6	04/04/11	Instruction Sets and Design	Laboratory
7	11/04/11	I/O, Interrupts, DMA	Tutorial
8	18/04/11	Cache Organisation	Laboratory
Mid semester break			
9	02/05/11	Mass Storage/Memory Management	Tutorial
10	09/05/11	CPU Organisation/Pipelined Architectures	Laboratory
11	16/05/11	Superscalar Architectures	Tutorial
12	23/05/11	CISC, RISC, VLIW, Other Machine Architectures	Laboratory
	30/05/11	SWOT VAC	No formal assessment is undertaken SWOT VAC

*Please note that these dates may only apply to Australian campuses of Monash University. Off-shore students need to check the dates with their unit leader.

Assessment Policy

To pass a unit which includes an examination as part of the assessment a student must obtain:

- 40% or more in the unit's examination, and
- 40% or more in the unit's total non-examination assessment, and
- an overall unit mark of 50% or more.

If a student does not achieve 40% or more in the unit examination or the unit non-examination total assessment, and the total mark for the unit is greater than 50% then a mark of no greater than 49-N will be recorded for the unit

Assessment Tasks

Participation

6 Laboratory Exercises each worth 5% of the total mark (compulsory and assessed, preparation required)

6 Tutorial Exercises each worth 1.667% of the total mark (compulsory and assessed)

Tutorials and Laboratories are scheduled in alternating weeks

- **Assessment task 1**

  Title:
  Laboratory Exercises
  Description:
  6 Laboratory Exercises
  Weighting:
  5% of total mark each
  Criteria for assessment:
  Compulsory. Preparation required. Individual assessment per task.

  The criteria used to assess laboratory tasks are:

  1. All programs must assemble and execute correctly. Evidence of testing is required.
  2. Programs must meet the problem specification.
  3. Assembly code should be readable and maintainable.
  4. Programs should be documented.
  5. All algorithms should follow the style presented in laboratory examples and be correct.
  6. Logic simulator circuits must comply with the specified truth table or other functional definition.

  Due date:
  In weeks 2,4,6,8,10 and 12

- **Assessment task 2**

  Title:
  Tutorial Exercises
  Description:
  6 Tutorial Exercises
  Weighting:
  Total 10%; 1.667% each
  Criteria for assessment:
  Compulsory.

  The criteria used to assess submissions are:

  1. Correctness and understanding - there may be more than one "right" answer in many cases. We will look for answers that reflect understanding of the underlying principles and theories.
  2. Completeness - that you have answered all parts of each question. Presentation - that you have presented your answers in a suitably formatted style.
  3. Use of evidence and argument - you are able to explain your position by using logical argument drawing on the theory presented in the unit.

  Due date:
  In weeks 1,3,5,7,9 and 11

Examinations

- **Examination 1**

Weighting:
60%
Length:
3 hours
Type (open/closed book):
Closed book
Electronic devices allowed in the exam:
Non programmable scientific calculators permitted

Assignment submission

Assignment coversheets are available via "Student Forms" on the Faculty website:
http://www.infotech.monash.edu.au/resources/student/forms/
You MUST submit a completed coversheet with all assignments, ensuring that the plagiarism declaration section is signed.

Extensions and penalties

Submission must be made by the due date otherwise penalties will be enforced.

You must negotiate any extensions formally with your campus unit leader via the in-semester special consideration process:
http://www.infotech.monash.edu.au/resources/student/equity/special-consideration.html.

Returning assignments

Students can expect assignments to be returned within two weeks of the submission date or after receipt, whichever is later

Policies

Monash has educational policies, procedures and guidelines, which are designed to ensure that staff and students are aware of the University's academic standards, and to provide advice on how they might uphold them. You can find Monash's Education Policies at:
http://policy.monash.edu.au/policy-bank/academic/education/index.html

Key educational policies include:

- Plagiarism (http://www.policy.monash.edu/policy-bank/academic/education/conduct/plagiarism-policy.html)
- Assessment (http://www.policy.monash.edu/policy-bank/academic/education/assessment/assessment-in-coursework-po
- Special Consideration (http://www.policy.monash.edu/policy-bank/academic/education/assessment/special-consideration-policy.h
- Grading Scale (http://www.policy.monash.edu/policy-bank/academic/education/assessment/grading-scale-policy.html)

- Discipline: Student Policy (http://www.policy.monash.edu/policy-bank/academic/education/conduct/student-discipline-policy.html)
- Academic Calendar and Semesters (http://www.monash.edu.au/students/key-dates/);
- Orientation and Transition (http://www.infotech.monash.edu.au/resources/student/orientation/); and
- Academic and Administrative Complaints and Grievances Policy (http://www.policy.monash.edu/policy-bank/academic/education/management/complaints-grievance-policy.

Student services

The University provides many different kinds of support services for you. Contact your tutor if you need advice and see the range of services available at www.monash.edu.au/students The Monash University Library provides a range of services and resources that enable you to save time and be more effective in your learning and research. Go to http://www.lib.monash.edu.au or the library tab in my.monash portal for more information. Students who have a disability or medical condition are welcome to contact the Disability Liaison Unit to discuss academic support services. Disability Liaison Officers (DLOs) visit all Victorian campuses on a regular basis

- Website: http://adm.monash.edu/sss/equity-diversity/disability-liaison/index.html;
- Telephone: 03 9905 5704 to book an appointment with a DLO;
- Email: dlu@monash.edu
- Drop In: Equity and Diversity Centre, Level 1 Gallery Building (Building 55), Monash University, Clayton Campus.

READING LIST

Recommended Reading:

William Stallings, Computer Organization and Architecture: Designing for Performance, 8/E, Prentice Hall, ISBN-13: 9780136073734

Morris Mano and Charles Kime , Logic and Computer Design Fundamentals 4/E, Pearson Prentice Hall, ISBN 0-13-140539-X

Supplementary Recommended Reading:

http://www.csse.monash.edu.au/~carlo/SYSTEMS/