MONASH University
Information Technology

FIT2069
Computer architecture

Unit Guide

Semester 1, 2015

Last updated: 24 Feb 2015

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FIT2069 Computer architecture - Semester 1, 2015

This unit covers the internal mechanism of computers and how they are organised and programmed. Topics include combinatorial and sequential logic, Boolean Algebra, Karnaugh maps, counters, ripple adders, tree adders, memory/addressing, busses, speed, DMA, data representation, machine arithmetic, microprogramming, caches and cache architectures, virtual memory and translation look-aside buffers, vectored interrupts, polled interrupts, pipelined architecture, superscalar architecture, data dependency, hazards, CISC, RISC, VLIW machine architectures.

Mode of Delivery

Clayton (Day)

Workload Requirements

Minimum total expected workload equals 12 hours per week comprising:

(a.) Contact hours for on-campus students:

- Two hours of lectures
- One 3-hour laboratory or one 2-hour tutorial (alternating weeks)

(b.) Additional requirements (all students):

- A minimum of 7-8 hours independent study per week for preparing for and completing lab and project work, private study and revision.

See also Unit timetable information

Additional workload requirements

This is a technically oriented unit where content in any given week depends strongly on content in preceding weeks. Therefore students should plan and commit the minimum specified hours for personal study every week. Laboratory work will require preparation before attendance.

The unit content requires a strong focus on understanding content through the semester.

Unit Relationships

Prerequisites

FIT1031 or FIT1001 and FIT1008 or FIT1015

Chief Examiner

Dr Carlo Kopp

Campus Lecturer

Clayton

Dr Carlo Kopp

Consultation hours: By appointment

Your feedback to Us

Monash is committed to excellence in education and regularly seeks feedback from students, employers and staff. One of the key formal ways students have to provide feedback is through the Student Evaluation of Teaching and Units (SETU) survey. The University's student evaluation policy requires that every unit is evaluated each year. Students are strongly encouraged to complete the surveys. The feedback is anonymous and provides the Faculty with evidence of aspects that students are satisfied and areas for improvement.

For more information on Monash's educational strategy, see:

www.monash.edu.au/about/monash-directions/ and on student evaluations, see:
www.policy.monash.edu/policy-bank/academic/education/quality/student-evaluation-policy.html

Previous Student Evaluations of this Unit

In response to the last SETU of this unit, the following changes have been made:

- Additional examples of real world hardware will be added into the lecture slides;
- Additional supplementary reading will be added;

Student feedback has highlighted the following strength(s) in this unit:

- *"I really liked how cohesive all the topics in this unit were. 10/10 unit."*
- *"Interesting subject matter, well structured and clearly refined over the years. Labs are challenging and useful. Having no assignments is great and makes sense in this unit."*
- *"The content is introduced at a proper pace and each lecture builds on the previous one so the students don't feel overwhelmed by having to absorb a large amount of information in one go."*
- *"The practicals were interesting and relevant The lectures were interesting and well explained. Good use of real world examples in lectures"*

If you wish to view how previous students rated this unit, please go to
https://emuapps.monash.edu.au/unitevaluations/index.jsp

Academic Overview

Learning Outcomes

At the completion of this unit students will have -A knowledge and understanding of:

- combinatorial and sequential logic, Boolean Algebra, Karnaugh maps, and hazards;
- counters, ripple adders, tree adders, memory/addressing, computer busses, logic and bus speed, and Direct Memory Access;
- data representation for integers and floating point operands;
- machine arithmetic, microprogramming;
- storage hierarchies, caches and cache architectures, performance impact of caching;
- virtual memory and translation look-aside buffers, performance impact of TLB caching;
- vectored and polled interrupt handling;
- pipelined architecture, superscalar architecture, data dependency, and hazards;
- CISC, RISC, VLIW machine architectures.

Developed the skills to:

- model combinatorial and sequential logic circuits using a simulator tool;
- perform programming tasks in assembly code.

Unit Schedule

Week	Activities	Assessment
0		No formal assessment or activities are undertaken in week 0
1	Intro/History/Background; Boolean Algebra	Tutorial 1
2	Karnaugh maps, Hazards; Data Representation	Laboratory 1
3	Counters, Adders, Shifters, Sequential Logic	Tutorial 2
4	Basic Machine Organisation	Laboratory 2
5	Control Unit Design	Tutorial 3
6	Instruction Sets and Design	Laboratory 3
7	I/O, Interrupts, DMA	Tutorial 4
8	Cache Organisation	Laboratory 4
9	Mass Storage/Memory Management	Tutorial 5
10	CPU Organisation/Pipelined Architectures	Laboratory 5
11	Superscalar Architectures	Tutorial 6
12	CISC, RISC, VLIW, Other Machine Architectures	Laboratory 6
	SWOT VAC	No formal assessment is undertaken in SWOT VAC
	Examination period	LINK to Assessment Policy: http://policy.monash.edu.au/policy-bank/academic/education/assessment/assessment-in-coursework-policy.html

*Unit Schedule details will be maintained and communicated to you via your learning system.

Teaching Approach

- **Lecture and tutorials or problem classes**
  This teaching and learning approach provides facilitated learning, practical exploration and peer learning.
- **Laboratory-based classes**
  This teaching approach is practical learning.

Assessment Summary

Examination (3 hours): 60%; In-semester assessment: 40%

Assessment Task	Value	Due Date
Laboratory Exercises	Total 30% (5% each)	Weeks 2, 4, 6, 8, 10 and 12
Tutorial Exercises	Total 10% (1.667% each)	Weeks 1, 3, 5, 7, 9 and 11
Examination 1	60%	To be advised

Assessment Requirements

Assessment Policy

Faculty Policy - Unit Assessment Hurdles
(http://intranet.monash.edu.au/infotech/resources/staff/edgov/policies/assessment-examinations/assessment-hurd

Academic Integrity - Please see resources and tutorials at
http://www.monash.edu/library/skills/resources/tutorials/academic-integrity/

Assessment Tasks

Participation

There are 6 Tutorial Exercises each worth 1.667% of the total mark (assessed).

There are 6 Laboratory Exercises each worth 5% of the total mark (assessed, preparation required).

Tutorials and Laboratories are scheduled in alternating weeks.

Attendance is expected and strongly recommended. This unit is tightly integrated so if students miss a Tutorial or Laboratory they will have difficulty understanding later material.

- **Assessment task 1**

Title:
Laboratory Exercises
Description:
6 Laboratory Exercises. Individual assessment per task. Preparation required.

Attendance is expected and strongly recommended. This unit is tightly integrated so if students miss a Laboratory they will have difficulty understanding later material.
Weighting:
Total 30% (5% each)
Criteria for assessment:
The criteria used to assess laboratory tasks are:

1. All programs must assemble and execute correctly. Evidence of testing is required.
2. Programs must meet the problem specification.
3. Assembly code should be readable and maintainable.
4. Programs should be documented.
5. All algorithms should follow the style presented in laboratory examples and be correct.
6. Logic simulator circuits must comply with the specified truth table or other functional definition.

Due date:
Weeks 2, 4, 6, 8, 10 and 12

- **Assessment task 2**

Title:
Tutorial Exercises
Description:
6 Tutorial Exercises. Individual assessment per task.

Attendance is expected and strongly recommended. This unit is tightly integrated so if students miss a Tutorial they will have difficulty understanding later material.
Weighting:
Total 10% (1.667% each)
Criteria for assessment:
The criteria used to assess submissions are:

1. Correctness and understanding - there may be more than one "right" answer in many cases. We will look for answers that reflect understanding of the underlying principles and theories.
2. Completeness - that you have answered all parts of each question.
3. Presentation - that you have presented your answers in a suitably formatted style.
4. Use of evidence and argument - you are able to explain your position by using logical argument drawing on the theory presented in the unit.

Due date:
Weeks 1, 3, 5, 7, 9 and 11

Examinations

- **Examination 1**

Weighting:
60%
Length:
3 hours
Type (open/closed book):
Closed book
Electronic devices allowed in the exam:
Non-programmable scientific calculators will be permitted.

Learning resources

Monash Library Unit Reading List (if applicable to the unit)
http://readinglists.lib.monash.edu/index.html

Feedback to you

Types of feedback you can expect to receive in this unit are:

- Informal feedback on progress in labs/tutes
- Test results and feedback

Extensions and penalties

Submission must be made by the due date otherwise penalties will be enforced.

You must negotiate any extensions formally with your campus unit leader via the in-semester special consideration process: http://www.monash.edu.au/exams/special-consideration.html

Returning assignments

Students can expect assignments to be returned within two weeks of the submission date or after receipt, whichever is later.

Assignment submission

It is a University requirement (http://www.policy.monash.edu/policy-bank/academic/education/conduct/student-academic-integrity-managing-pla for students to submit an assignment coversheet for each assessment item. Faculty Assignment coversheets can be found at http://www.infotech.monash.edu.au/resources/student/forms/. Please check with your Lecturer on the submission method for your assignment coversheet (e.g. attach a file to the online assignment submission, hand-in a hard copy, or use an electronic submission). Please note that it is your responsibility to retain copies of your assessments.

Online submission

If Electronic Submission has been approved for your unit, please submit your work via the learning system for this unit, which you can access via links in the my.monash portal.

Recommended Resources

Software:

Logisim software (free)

Xspim/Spim software (free)

Supplementary Reading:

http://www.csse.monash.edu.au/~carlo/SYSTEMS/

Recommended text(s)

William Stallings. (). *Computer Organization and Architecture: Designing for Performance*. (8th Edition) Prentice Hall (ISBN: 13: 9780136073734).

Morris Mano and Charles Kime. (). *Logic and Computer Design Fundamentals*. (4th Edition) Pearson Prentice Hall (ISBN: 0-13-140539-X).

Examination material or equipment

Non-programmable scientific calculators will be permitted.

Other Information

Policies

Monash has educational policies, procedures and guidelines, which are designed to ensure that staff and students are aware of the University's academic standards, and to provide advice on how they might uphold them. You can find Monash's Education Policies at:
www.policy.monash.edu.au/policy-bank/academic/education/index.html

Faculty resources and policies

Important student resources including Faculty policies are located at
http://intranet.monash.edu.au/infotech/resources/students/

Graduate Attributes Policy

http://www.policy.monash.edu/policy-bank/academic/education/management/monash-graduate-attributes-policy.h

Student Charter

www.opq.monash.edu.au/ep/student-charter/monash-university-student-charter.html

Student services

The University provides many different kinds of support services for you. Contact your tutor if you need advice and see the range of services available at http://www.monash.edu.au/students. For Malaysia see http://www.monash.edu.my/Student-services, and for South Africa see http://www.monash.ac.za/current/.

Monash University Library

The Monash University Library provides a range of services, resources and programs that enable you to save time and be more effective in your learning and research. Go to www.lib.monash.edu.au or the library tab in my.monash portal for more information. At Malaysia, visit the Library and Learning Commons at http://www.lib.monash.edu.my/. At South Africa visit http://www.lib.monash.ac.za/.

Disability Liaison Unit

Students who have a disability or medical condition are welcome to contact the Disability Liaison Unit to discuss academic support services. Disability Liaison Officers (DLOs) visit all Victorian campuses on a regular basis.

- Website: http://www.monash.edu/equity-diversity/disability/index.html
- Telephone: 03 9905 5704 to book an appointment with a DLO; or contact the Student Advisor, Student Commuity Services at 03 55146018 at Malaysia
- Email: dlu@monash.edu
- Drop In: Equity and Diversity Centre, Level 1, Building 55, Clayton Campus, or Student Community Services Department, Level 2, Building 2, Monash University, Malaysia Campus

Other

Engineers Australia Stage 1 competencies

This unit is a core unit in the Bachelor of Software Engineering accredited by Engineers Australia. Engineers Australia Accreditation Policy of Professional Engineering Programs requires that programs demonstrate how engineering graduates are prepared for entry to the profession and achieve Stage 1 competencies. The following information describes how this unit contributes to the development of these competencies for the Bachelor of Software Engineering. (Note: not all competencies may be emphasised in this unit).

Stage 1 competency	**How the compency is developed in this unit**
1. Knowledge and Skills base	
1.1. **Comprehension, theory based understanding** of the underpinning natural and physical sciences and the engineering fundamentals applicable to the engineering discipline.	The unit covers many aspects of computing fundamentals and foundations which underpins the software engineering discipline.
1.2. **Conceptual understanding** of the mathematics, numerical analysis, statistics, and computer and information sciences, which underpin the engineering discipline.	The unit covers the concepts of computer architecture and its components underpinning the software engineering discipline. Students have the opportunity to investigate, model, design and analyse various aspects of computer architecture in the unit assessment.
1.3. **In-depth understanding** of specialist bodies of knowledge within the engineering discipline.	Not covered in this unit.
1.4. **Discernment** of knowledge development and research directions within th engineering discipline.	Not covered in this unit.
1.5. **Knowledge** of engineering design practice and contextual factors impacting the engineering discipline.	Not covered in this unit.
1.6. **Understanding** of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline.	Not covered in this unit.
2. Engineering application ability	
2.1. **Application** of established engineering methods to complex engineering problem solving.	Not covered in this unit.
2.2 **Fluent application** of engineering techniques, tools and resources.	Not covered in this unit.
2.3. **Application** of systematic engineering synthesis and design processes.	Not covered in this unit.
2.4. **Application** of systematic approaches to the conduct and management of engineering projects.	Not covered in this unit.
3. Professional and personal attributes	
3.1. **Ethical** conduct and professional accountability.	Not covered in this unit.
3.2. **Effective** oral and written communication in professional and lay domains.	Students in tutorials and labs must explain their work to the tutors/demonstrators, as well as provide their solutions in writing.
3.3. **Creative**, innovative and proactive demeanour.	Developing solutions for lab and tutorial exercises is inherently a creative endeavour.

3.4. **Professional** use and management of information.	Not covered in this unit.
3.5. **Orderly** management of self, and professional conduct.	Not covered in this unit.
3.6. **Effective** team membership and team leadership.	Not covered in this unit.

Relationship between Unit Learning Outcomes and BSE Course Outcomes

No.	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	CO 7	C0 8	CO 9	CO 10	CO 11	CO 12	CO 13
1	X												
2	X							X					X
3	X							X					X
4	X												
5	X												

Relationship between Unit Learning Outcomes and Assessments

No.	Assignments	Tests	Practical Exercises	Exam
1			X	X
2			X	X
3			X	X
4			X	
5			X	